AMENDMENTS TO THE CLAIMS

1. (Currently amended): A method for synchronizing a plurality of digital input signals, which are formed by sampling with a dedicated operating clock in each case, comprising:

forming digital auxiliary signals by sampling the digital input signals with a ~~common~~ post-processing clock, which is at least twice as fast as the fastest operating clock and which is generated by only one resampling device; and

forming synchronized digital output signals which correspond to the digital input signals by interpolating each digital auxiliary signal.

2. (Previously presented): The method as claimed in claim 1, further comprising:

before sampling the common post-processing clock, filtering the digital input signals with a filter having a characteristic which is an inverse of a characteristic of an interpolation filter used for interpolating.

3. (Previously presented): The method as claimed in claim 1, further comprising:

filtering the synchronized digital output signals with an anti-aliasing filter directly after the interpolation.

4. (Previously presented): The method as claimed in claim 1, wherein

the digital input signals are obtained from secondary variables, sampled with a dedicated operating clock, of measuring transducers in an electric power supply system.

5. (Previously presented): The method as claimed in claim 4, further comprising:

in the case of digital input signals formed from secondary variables of Rogovsky measuring transducers, the digital auxiliary signals are formed directly from the input signals, and an integrator is used for the interpolation.